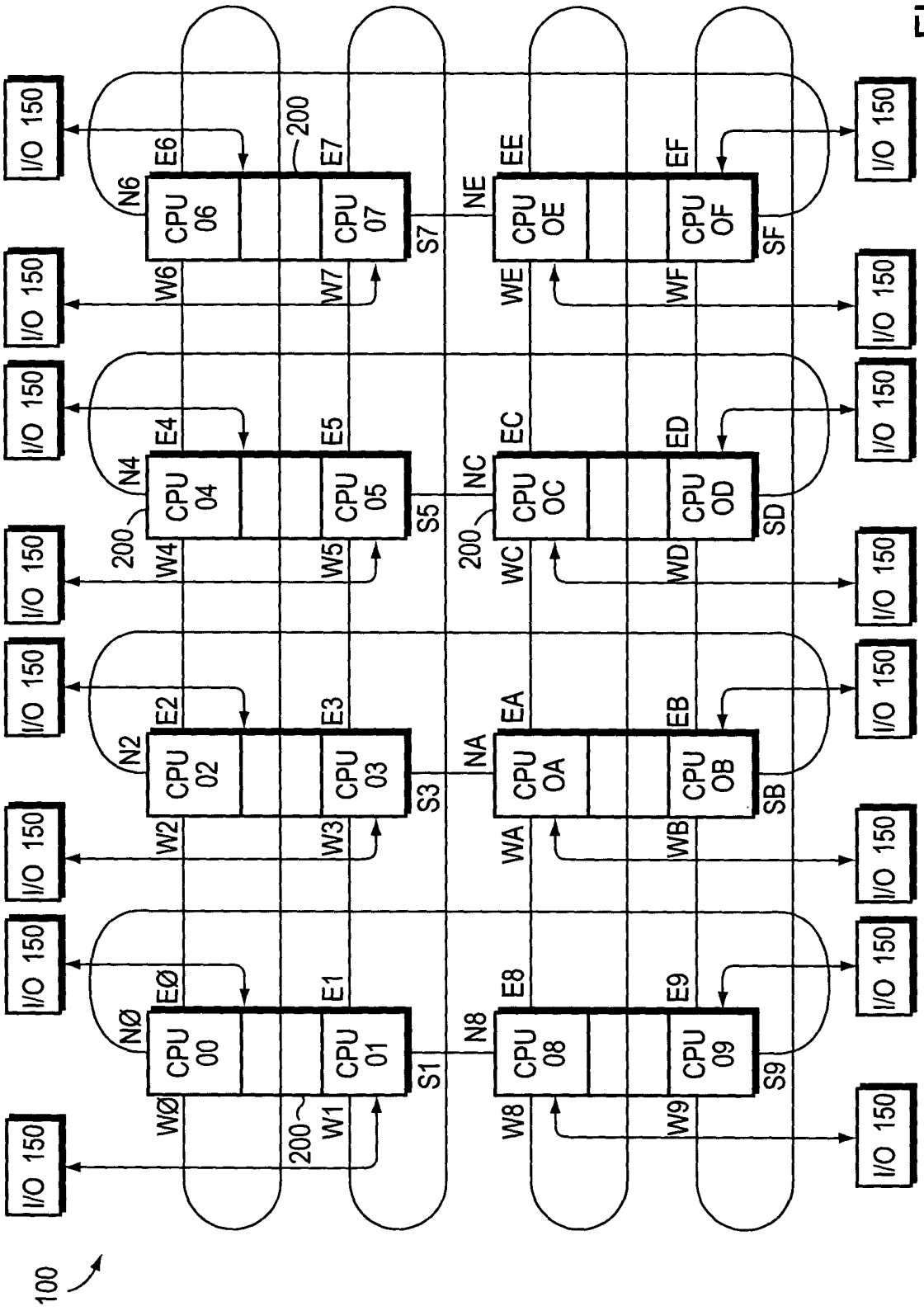
100
I/O 150
200
CPU 00
CPU 01
CPU 02
CPU 03
CPU 04
CPU 05
CPU 06
CPU 07
CPU 08
CPU 09
CPU 0A
CPU 0B
CPU 0C
CPU 0D
CPU 0E
CPU 0F
NØ
N2
N4
N6
N8
NA
NC
NE
EØ
E1
E2
E3
E4
E5
E6
E7
E8
E9
EA
EB
EC
ED
EE
EF
WØ
W1
W2
W3
W4
W5
W6
W7
W8
W9
WA
WB
WC
WD
WE
WF
S1
S3
S5
S7
S9
SB
SD
SF

FIG. 1

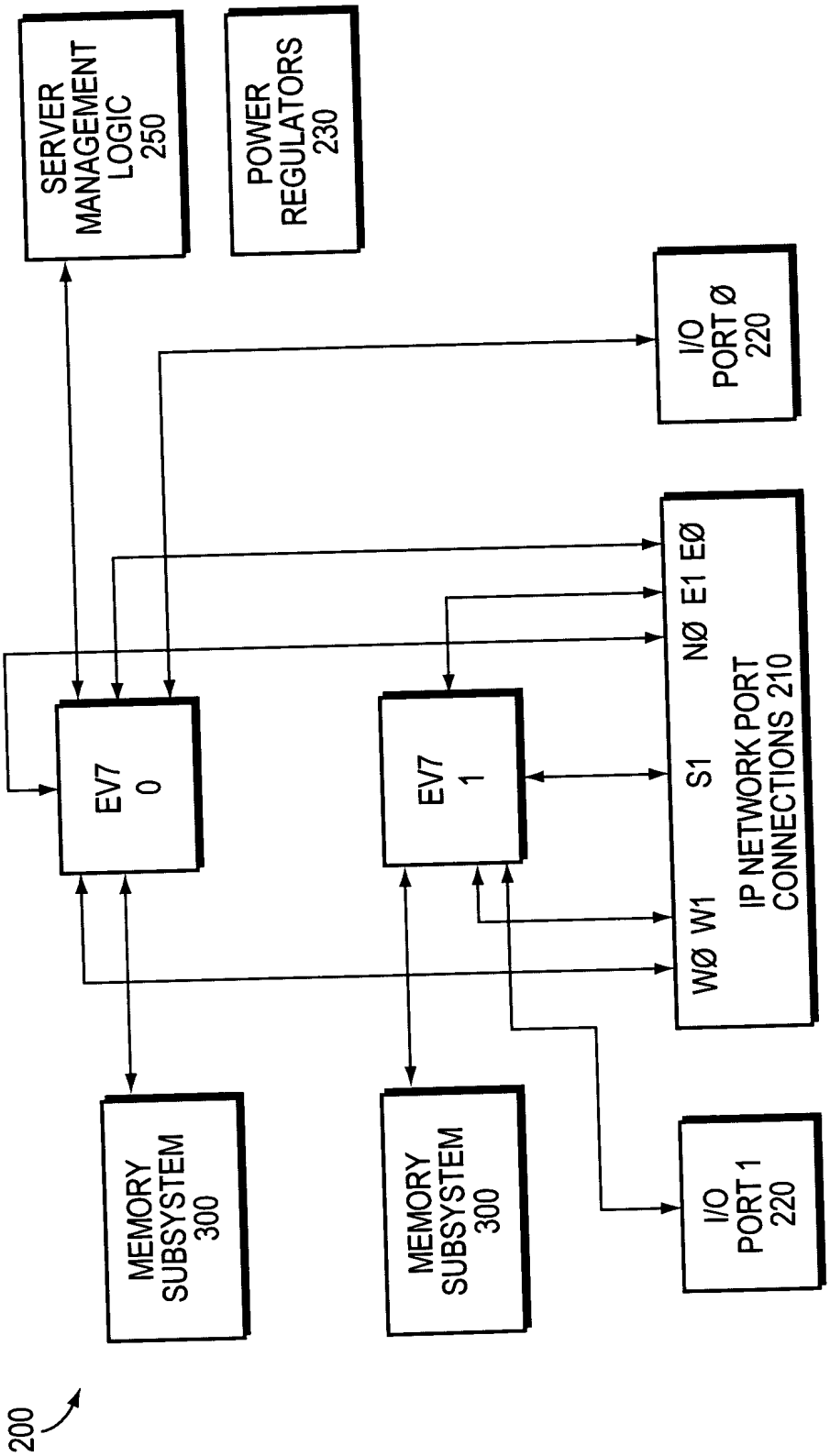
SERVER MANAGEMENT LOGIC 250
POWER REGULATORS 230
I/O PORT Ø 220
EV7 0
EV7 1
NØ E1 EØ
S1
IP NETWORK PORT CONNECTIONS 210
WØ W1
MEMORY SUBSYSTEM 300
MEMORY SUBSYSTEM 300
I/O PORT 1 220
200

FIG. 2

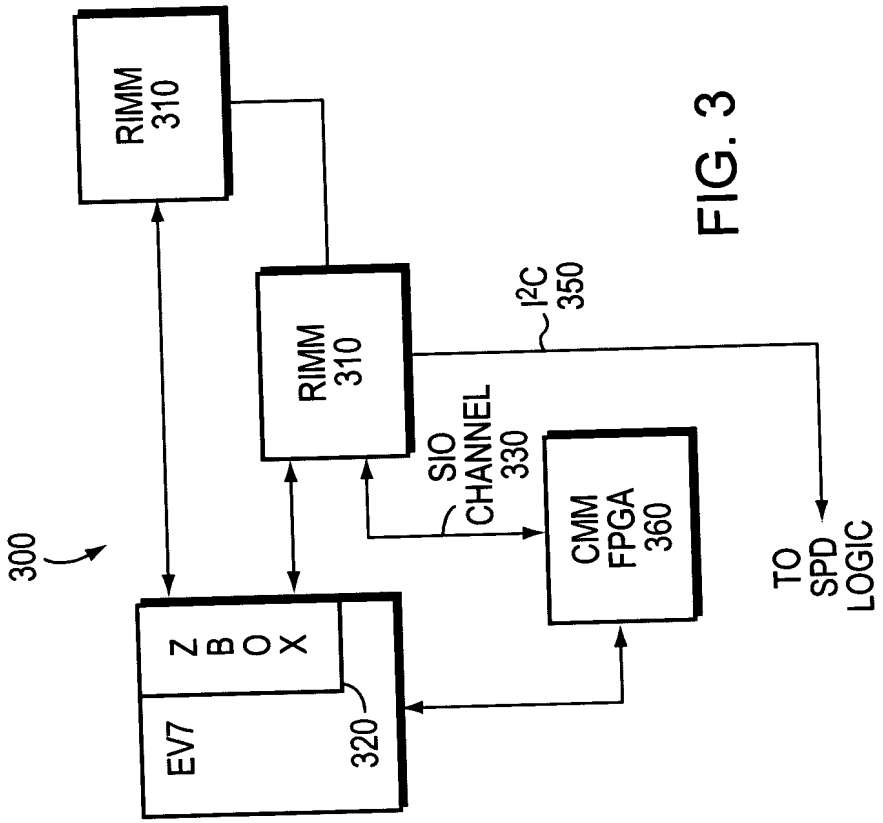
RIMM
310
RIMM
310
I2C
350
SIO
CHANNEL
330
CMM
FPGA
360
TO
SPD
LOGIC
300
EV7
ZBOX
320

FIG. 3

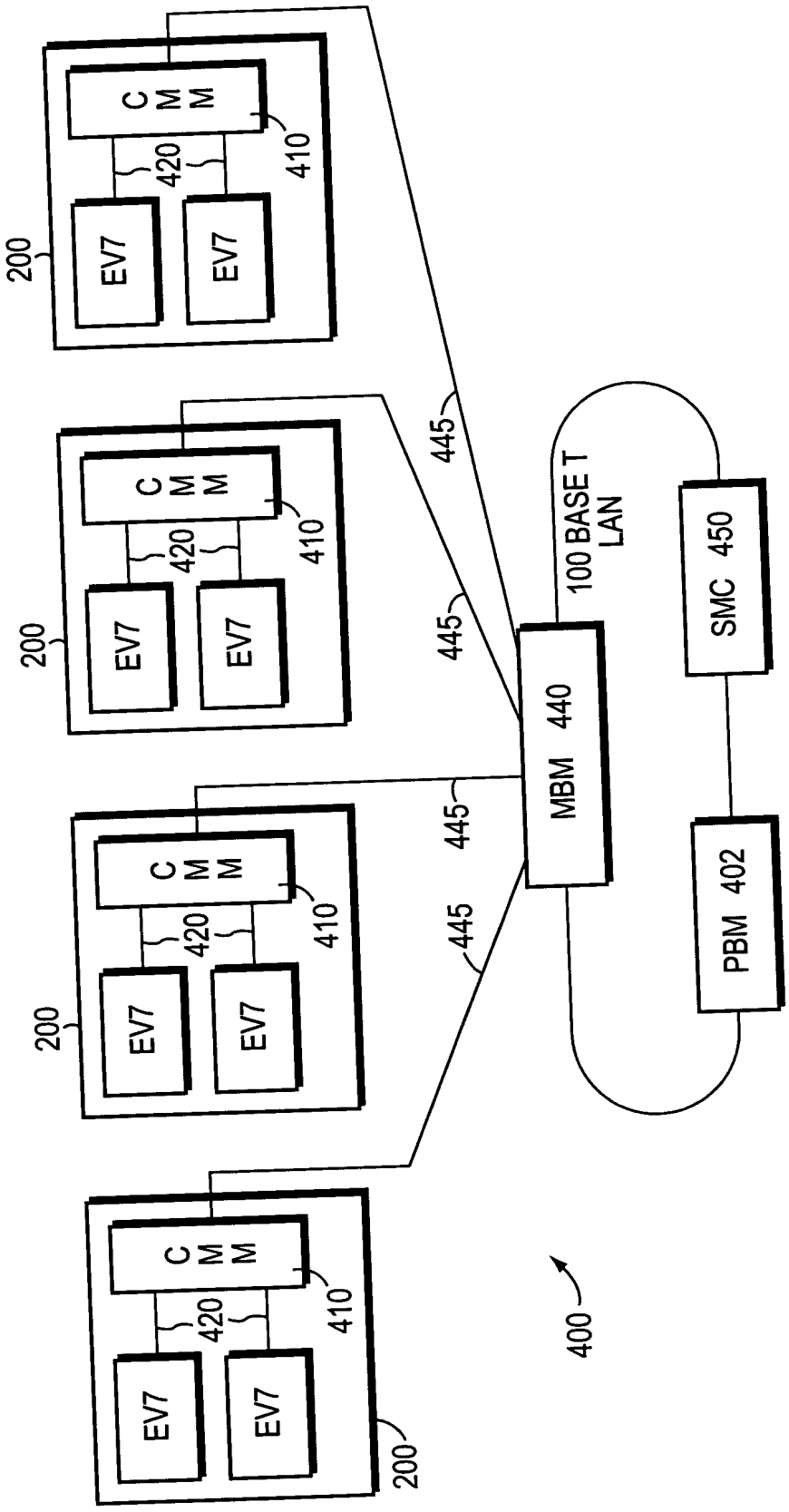
200
EV7
EV7
C M M
420
410
445
MBM 440
100 BASE T LAN
SMC 450
PBM 402
400

FIG. 4

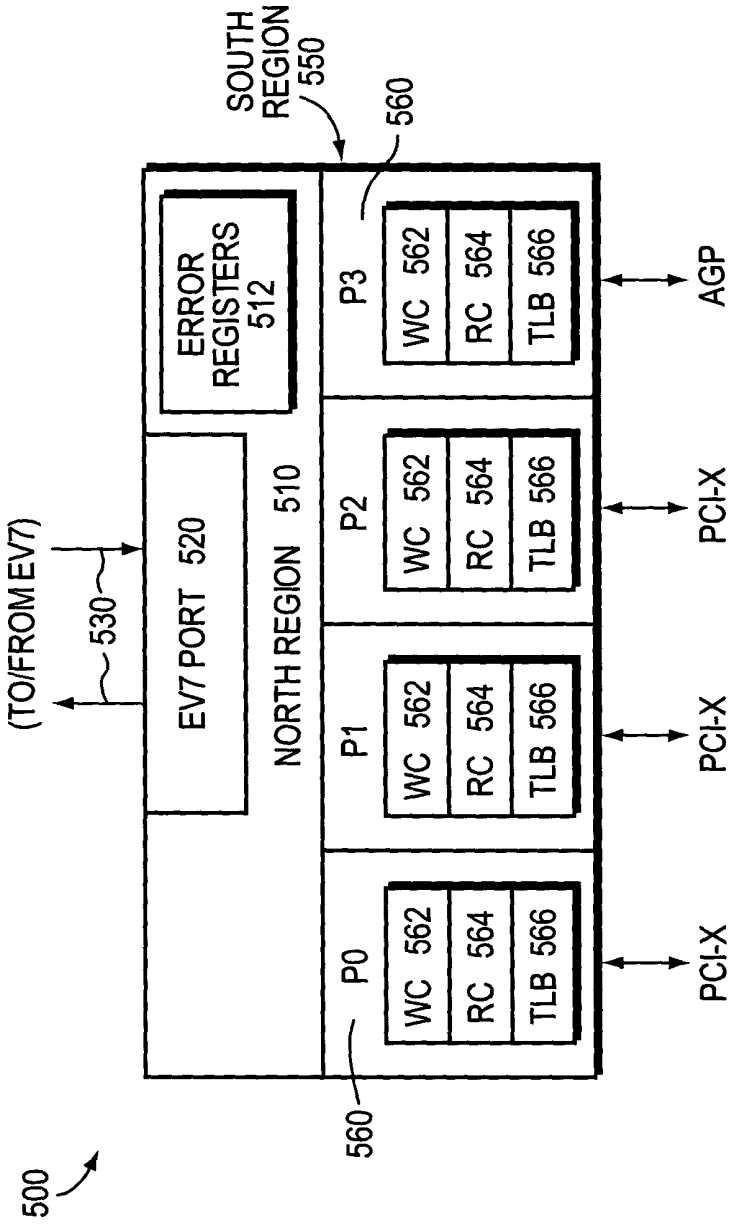
500
(TO/FROM EV7)
530
EV7 PORT 520
NORTH REGION 510
ERROR REGISTERS 512
SOUTH REGION 550
560
P3
P2
P1
P0
WC 562
RC 564
TLB 566
AGP
PCI-X
PCI-X
PCI-X
560

FIG. 5

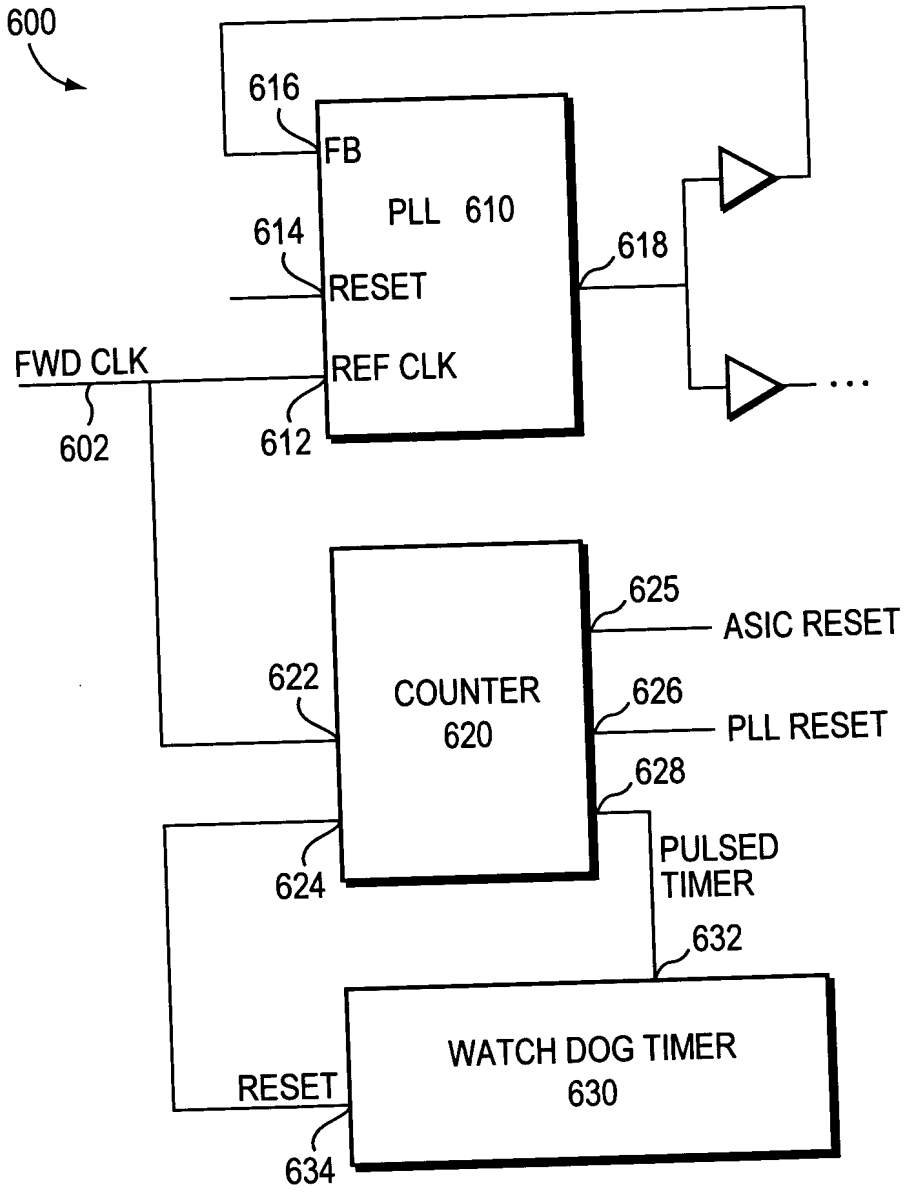
600
616
FB
PLL 610
614
RESET
618
FWD CLK
REF CLK
602
612
625
ASIC RESET
622
COUNTER
620
626
PLL RESET
628
624
PULSED
TIMER
632
WATCH DOG TIMER
630
RESET
634

FIG. 6